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A METHOD TO FORM A METAL SILICIDE GATE DEVICE

BACKGROUND OF THE INVENTION

(1) Field of the Invention

The invention relates to integrated circuit manufacturing, and, more particularly, to a method to fabricate a metal silicide gate device in the manufacture of an integrated circuit device.

(2) Description of the Prior Art

Metal-oxide-semiconductor (MOS) devices are commonly used in the art of integrated circuits. MOS devices offer many advantages over, for example, bipolar devices, such as the ability to form millions of such devices on the surface of the integrated circuit and the very low gate current of these devices. In a typical, high density MOS product, the gate terminal is fabricated using polysilicon. This choice provides many benefits from a manufacturing and device standpoint. However, as device and feature sizes have continued to be reduced, the inherent disadvantages of polysilicon have received increased attention. When compared to a metal material,

polysilicon has a relatively high resistivity. In a very small MOS device, or in a very high-speed application, the gate resistance, even of heavily doped polysilicon, can adversely limit the device performance. In addition, polysilicon inherently causes a depletion effect that must be compensated for using the threshold implant. This depletion effect further limits the application of polysilicon for the gate terminal material in very low supply voltage products.

The are several approaches in the art to improving the performance of the MOS transistor device by altering or replacing the polysilicon material. One approach is to replace the polysilicon layer with a metal layer as is shown in the process sequence illustrated in Figs. 1 through 4. Referring specifically to Fig. 1, a partially completed integrated circuit device is shown in a cross sectional representation. The device comprises, at this point in the fabrication process, a semiconductor substrate 10 onto which are formed a series of temporary gates. Each gate is formed by a patterned polysilicon layer 18 overlying the substrate 10 with a dielectric layer 14 therebetween. Further processing has been performed to form source and drain regions 22. Spacers 26 have been formed as part of the lightly doped drain (LDD) and heavily doped source/drain system as is well-known in the art. A masking or capping layer

30 is formed overlying each polysilicon gate 18. An isolation layer 34 is formed overlying the substrate 10 and electrically isolating each gate.

At this stage in the process, the cross-section shows typical MOS devices with polysilicon gates 18. However, in this case, the gates 18 are temporary and serve to form the boundaries for permanent metal gates that will be formed by a damascene process. Referring now to Fig. 2, the capping layer 30, polysilicon layer 18, and dielectric layer 14 are completely removed to reveal gate openings 38. Referring now to Fig. 3, these openings are then filled by, first, forming a new dielectric layer 42 on the surface of the substrate 10 in the gate openings. Next, a metal layer 46, is deposited to fill the gate openings. Finally, referring now to Fig. 4, the metal layer 46 is polished down to remove the excess metal 46 between the gates and to thereby confine the metal layer 46 to the gate openings. The resulting metal gates 46 exhibit improved performance over the polysilicon gates, especially in dramatically reduced gate resistance. However, the process requires that the gate dielectric layer be re-formed and requires a polishing operation.

Several prior art inventions relate to silicide gate methods and devices. U.S. Patent 6,465,309 B1 to Xiang et al describes a method to form a silicide gate transistor. An amorphous silicon layer is deposited following complete removal of a temporary polysilicon gate. U.S. Patent 6,475,908 B1 to Lin et al describes a method to form metal silicide gate MOS transistors. In one embodiment, a temporary gate is formed and then removed. A metal/oxide gate is then formed in the opening. The metal is converted to silicide by ion implantation of silicon ions and thermal processing. U.S. Patent 6,528,402 B2 to Tseng describes a method to form a self-aligned, silicide gate. A polysilicon gate is partially converted to metal silicide.

SUMMARY OF THE INVENTION

A principal object of the present invention is to provide an effective and very manufacturable method to form a metal silicide gate MOS device.

A further object of the present invention is to provide a metal silicide gate MOS process that does not require re-forming the gate dielectric.

A yet further object of the present invention is to provide a metal silicide gate MOS process that follows the damascene metal interconnect process.

A yet further object of the present invention is to provide a metal silicide gate MOS process that is easily compatible with a dual thickness, gate oxide process.

A yet further object of the present invention is to provide a metal silicide gate MOS process that does not require a metal polishing process.

A yet further object of the present invention is to provide a metal silicide gate MOS process that allows the threshold implant to easily adjust the voltage threshold for CMOS devices, even in very low voltage systems.

Another further object of the present invention is to provide a metal silicide gate MOS device with improved performance.

In accordance with the objects of this invention, a method to form metal silicide gates in the fabrication of an integrated circuit device is achieved. The method comprises forming

polysilicon lines overlying a substrate with a dielectric layer therebetween. A first isolation layer is formed overlying the substrate and the sidewalls of the polysilicon lines. The first isolation layer does not overlie the top surface of the polysilicon lines. The polysilicon lines are partially etched down such that the top surfaces of the polysilicon lines are below the top surface of the first isolation layer. A metal layer is deposited overlying the polysilicon lines. A thermal anneal is used to completely convert the polysilicon lines to metal silicide gates. The unreacted metal layer is removed to complete the device.

Also in accordance with the objects of this invention, a metal silicide gate MOS device is achieved. The device comprises a metal silicide gate overlying a substrate with a dielectric layer therebetween. Spacers are on the sidewalls of the metal silicide gate. The spacers are substantially taller than the metal silicide gate.

BRIEF DESCRIPTION OF THE DRAWINGS

In the accompanying drawings forming a material part of this description, there is shown:

Figs. 1 through 4 illustrate a prior art method of forming a metal gate MOS device.

Figs. 5 through 18 illustrate a preferred embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The preferred embodiments of the present invention disclose a method to form a metal silicide gate MOS device in the manufacture of an integrated circuit device. A polysilicon gate is partially etched away and, then, is converted to metal silicide. It should be clear to those experienced in the art that the present invention can be applied and extended without deviating from the scope of the present invention.

Figs. 5 through 18 illustrate a preferred embodiment of the present invention. Several important features of the present invention are shown and discussed below. Referring particularly to Fig. 5, a cross-section of a partially completed integrated circuit device is illustrated. A substrate 50 is provided. The substrate 50 preferably comprises a semiconductor material and, more preferably, comprises monocrystalline silicon as is well-known in the art. The semiconductor material 50 may further be

doped with impurity ions such that the resulting substrate is n-type or p-type.

A dielectric layer 54a and 54b is formed overlying the substrate 50. The dielectric layer 54a and 54b comprises an insulator material. Preferably, an oxide is used for the dielectric. Most preferably, the dielectric layer 54a and 54b comprises silicon oxide that is grown overlying a silicon substrate 50 by a thermal process. Alternatively, a silicon oxide layer 54a and 54b may be deposited by a chemical vapor deposition (CVD) process using a precursor. Other insulators, such as metal oxides or metal nitride oxides, could also be used. In the particular illustration, the dielectric layer 54a and 54b is shown to possess two thicknesses. Where an integrated circuit device is formed having an especially thin gate dielectric layer 54a in the core logic/processing circuits, it is sometimes advantages to form a thicker dielectric layer 54b in the input/output (I/O) sections. In this way, very high speed MOS transistors can be formed in the CORE using the thinner dielectric 54a while higher voltage capable MOS transistors can be formed in the I/O using the thicker dielectric 54b. Many schemes have been proposed to form multiple thickness gate dielectrics in the art. The use of multiple dielectric thickness is given as an example of a useful application of the present

invention but is not a critical or necessary component of the present invention.

Referring now to Fig. 6, a polysilicon layer 58 is formed overlying the dielectric layer 54a and 54b. The polysilicon layer 58 is preferably formed by CVD or by low-pressure CVD. The polysilicon layer 58 preferably has a thickness of between about 200 Å and about 5,000 Å. The polysilicon layer 58 is important because the polysilicon 58 is partially etched down prior to conversion to metal silicide. Hence, the polysilicon layer 58 must be made thick enough to not be etched through by this later etching step. The polysilicon layer 58 may be formed doped or undoped though the later, complete conversion to metal silicide will cause any doping effect to be moot in establishing the gate resistance.

A hard mask layer 62 is deposited overlying the polysilicon layer 58. The hard mask layer 62 is used for patterning the polysilicon 58 and for protecting the top surface of the polysilicon 58 during subsequent processing. The hard mask layer 62 comprises a material that can be selectively etched with respect to the polysilicon layer 58. Preferably, silicon nitride is deposited by a CVD process to form the hard mask layer 62.

The hard mask layer 62 is preferably formed to a thickness of between about 100 Å and about 1,000 Å.

Referring now to Fig. 7, the hard mask layer 62 is patterned. This patterning step is preferably performed using a patterned photoresist layer 72. For example, a photoresist layer 72 may be applied overlying the hard mask layer 62. The photoresist layer 72 is then exposed to actinic light through a mask to cause part of the photoresist polymer 72 to become cross-linked while part remains non-cross-linked. The photoresist 72 is then developed to cause part of the photoresist 72 to be washed away while part remains as the transferred pattern of the mask. The hard mask layer 62 is etched using the patterned photoresist layer 72 as a mask such that the pattern is transferred to the hard mask layer. The etching step may be performed using a wet chemical or dry chemical etch as is well-known in the art. The photoresist layer 72 is stripped away after the hard mask etch.

Referring now to Fig. 8, an important feature of the present invention is illustrated. The polysilicon layer 58 is patterned to form the gates for the planned MOS devices. The patterned hard mask layer 62 is used to mask the etching process such that the pattern is transferred from the hard mask layer 62

to the polysilicon layer 58. A wet or dry etching process may be used, though it is preferred that the polysilicon layer 58 is etched using a dry etch such as a reactive ion etch (RIE) as is known in the art. The etching process may remove a part of the hard mask layer 62 to cause the rounded shape as seen.

Referring now to Fig. 9, ions are implanted 66 to form first doped regions 70 in the substrate 50. The patterned polysilicon lines 58 block the implantation of ions into the substrate 50 under these lines 58. In this way, the first doped regions 70 are formed adjacent to, or self-aligned to, the polysilicon lines 58. The first doped regions 70 preferably are lightly doped to the opposite type of the substrate 50 and correspond to lightly doped drains (LDD) as are well-known in the art.

Referring now to Fig. 10, spacers 74 are then formed on the sidewalls of the polysilicon lines 58. The spacers 74 comprise an insulator material, such as oxide or nitride. Preferably, the spacers 74 comprise silicon nitride. The spacers 74 may be formed, for example, by depositing the spacer film overlying the substrate 50 and the polysilicon lines 58. An anisotropic etch is then performed to etch the spacers in the vertical direction until the spacer film is removed from the horizontal surfaces

leaving the spacers 74 adjacent to the edges of the polysilicon lines 58. The resulting spacers 74 have a width of between about 200 Å and about 1000 Å.

Referring now to Fig. 11, a second ion implantation 78 is performed. Ions are implanted 78 into the substrate 50 in the areas not blocked by the polysilicon lines 58 or the spacers 74. In this way, second doped regions 82 are formed adjacent to, or self-aligned to, the spacers 74. These second doped regions 82 correspond to source/drain regions and are preferably heavily doped to the opposite type of the substrate 50.

Referring now to Figs. 12 and 13, another important feature of the present invention is illustrated. To reduce the source/drain 82 resistance, a metal silicide layer 90 may be formed on the second heavily doped (source/drain) regions 82. Referring particularly to Fig. 12, a metal layer 86 is formed overlying the substrate 50. The metal layer 86 preferably comprises a metal that is reactive with silicon such as cobalt, nickel, or titanium. A thermal anneal is then performed to greatly increase the reaction rate between the silicon of the substrate 50 and the metal layer 86. The reaction product is metal silicide (MSi_x) as is well-known in the art. Referring particularly to Fig. 13, the metal silicide layer 90 only forms

on the exposed substrate 50 because the spacers 74 and hard mask layer 62 protect the polysilicon lines 58 from exposure to the reactive metal 86. The unreacted metal 86 is removed. At this point in the process, the polysilicon lines 58 have been used as place holders to align the formation of the source/drain regions 82, the LDD regions 70, the metal silicide regions 90, and the spacers 74.

Referring now to Fig. 14, a first isolation layer 98 is formed overlying the substrate 50 and providing an isolation between the polysilicon lines 58. Prior to the deposition of the first isolation layer 98, a contact stop layer 94 may be formed overlying the substrate 50, the spacers 74, and the hard mask layer 62. The contact stop layer 94 is used to provide an etch stop for the subsequent contact opening etch used in the metal interconnect processing. Preferably, the contact stop layer 94 comprises silicon nitride. The first isolation layer 98 preferably comprises an oxide layer, such as silicon oxide, that is deposited using a CVD process. Alternatively, spin-on glass or organic-based, low-k dielectrics could be used. The first isolation layer 98 is preferably formed to a substantial thickness such that the gaps between the polysilicon lines 58 are filled. The first isolation layer 98 may then be planarized to remove excess first isolation material 98 such that the

isolation layer 98 is confined to the gaps between the lines 98. A polishing operation, such as a chemical mechanical polish (CMP), may be used. The hard mask layer 62 protects the top surfaces of the polysilicon lines 58 from the planarization process and may act as a stopping mechanism for the planarization process as is well-known in the art.

Referring now to Fig. 15, an important feature of the present invention is illustrated. The polysilicon lines 58 are partially etched down such that the top surfaces of the resulting polysilicon lines 58' are below the top surface of the first isolation layer 98. The hard mask layer 62 is first removed by etching away. Then the polysilicon layer 58' is partially etched down. It is preferred that a dry etching process, selective to polysilicon, is used to etch the polysilicon down. In the preferred embodiment, the resulting polysilicon lines 58' are below the top surface of the first isolation layer by a distance D of between about 300 Å and about 1,000 Å. Alternatively, the remaining polysilicon lines 58' have a thickness of between about 100 Å and about 500 Å. Most importantly, the resulting polysilicon lines 58' cover and protect the dielectric layer 54a and 54b and are thin enough so that the subsequent silicide process will completely convert the lines to metal silicide.

Referring now to Fig. 16, another important feature of the present invention is illustrated. A metal layer 100 is deposited overlying the remaining polysilicon lines 58' and the first isolation layer 98. The metal layer 100 comprises a metal that will react with the polysilicon layer 58' to form metal silicide. Preferably, the metal layer 100 comprises cobalt or nickel and is deposited by physical vapor deposition (PVD). A thermal annealing operation is then performed to catalyze the reaction of the metal layer 100 and the polysilicon layer 58'. For example, the entire device can be thermally treated at a temperature of between about 150°C and about 800°C for between about 0.5 minutes and about 10 minutes. This treatment will cause the complete conversion of the polysilicon layer 58' into a metal silicide (MSi_x) layer 102 as shown in Fig. 17. The non-reacted metal layer 100 is then removed to complete the metal silicide gate 102 device. The resulting metal silicide gate electrodes 102 have a thickness of between about 100 Å and about 900 Å.

Referring now to Fig. 18, the device may be further processed by depositing a second isolation layer 106 overlying the metal silicide gates 102 and the first isolation layer 98. Contact openings are then patterned into the second isolation

layer 106. Another metal layer 110 is then deposited to fill the contact openings and patterned to form interconnecting lines.

Referring again to Fig. 17, the novel metal silicide gate MOS device may now be described. The device comprises a metal silicide gate 102 overlying a substrate 50 with a dielectric layer 54a and 54b therebetween. Spacers 74 are on the sidewalls of the metal silicide gate 102. The spacers 74 are substantially taller than the metal silicide gate 102. The device may further comprise source and drain regions 82 and lightly doped drain regions (LDD) 70. Metal silicide regions 90 may further be formed in the substrate 50 at the source and drain regions 82.

The advantages of the present invention may now be summarized. An effective and very manufacturable method to form a metal silicide gate MOS device is achieved. The metal silicide gate MOS process does not require re-forming the gate dielectric. The metal silicide gate MOS process follows the damascene metal interconnect process. The metal silicide gate MOS process is easily compatible with a dual thickness, gate oxide process. The metal silicide gate MOS process does not require a metal polishing process. The metal silicide gate MOS process allows the threshold implant to easily adjust the voltage threshold for CMOS devices, even in very low voltage

systems. The resulting metal silicide gate MOS device has improved performance by lowering the gate resistance.

As shown in the preferred embodiments, the novel method and device of the present invention provides an effective and manufacturable alternative to the prior art.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

What is claimed is: